REMARKS

Claims 1-31 are pending in this application. In the Office Action dated October 5, 2005, the Examiner took the following action: (1) objected to claim 8 for informalities; and (2) rejected claims 1-31 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 6,552,955 to Miki in view of U.S. Patent No. 6,449,209 to Lee.

The disclosed embodiments of the invention will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

The disclosed embodiment of the invention is a memory device having a plurality of memory banks, at least some of which are of different sizes, *i.e.*, they contain different numbers of memory cells. The memory device also includes a mode register that may be programmed to select the length of data bursts when the memory device is operating in a burst mode. Although the use of a mode register for this purpose in a memory device is conventional, the disclosed embodiment of the invention uses the mode register to select the bank to which data are to be written or from which data are to be read based upon the length of data burst programmed in the mode register. Therefore, as explained on page 7 of the application, if the mode register is programmed to access data with a long burst, the data can be accessed in a bank having a large number of columns. On the other hand, if the mode register is programmed to access data with a short burst, the data can be accessed from a bank having a small number of columns. As a result, programming the mode register to operate in a particular burst mode also programs the memory device to access memory banks having corresponding sizes, thereby ensuring efficient operation of the memory device.

The Examiner is complemented for his diligence in uncovering relevant prior art in this application. The patent to Lee found by the Examiner admittedly discloses a semiconductor memory device having a plurality of banks of different sizes. However, the Lee patent does not disclose using a mode register to select which bank is accessed based upon the

burst length programmed into the mode register. Instead, the Lee patent teaches using an external address to access one of several memory banks of different sizes. The addresses are, in turn, generated based upon the characteristics of various master devices accessing the memory device. The bank selected for access must therefore be determined by a device, such as a memory controller, that is external to the memory device based on the characteristics of the master devices requesting access to the memory device. In contrast, in the disclosed memory device, the bank selected for access is determined by programming the mode register with a burst length in the memory device itself. Therefore, a system using the disclosed memory device need not be specially adapted to address one of several banks of memory cells based upon the desired size of the memory bank. Instead, the disclosed memory device may be used in a system that is not specially adapted to address or otherwise select one of several memory banks based on the desired memory bank size. The system need only operate in a conventional manner to program a mode register to select the desired burst length.

The patent to Miki has been cited for disclosing a memory device having a mode register that is programmed to control the burst length at which the memory device operates. As acknowledged above, programming a mode register for this purpose is conventional. However, the burst length programmed into the mode register does not have any effect on which of several banks of memory are selected in the Miki memory device.

Turning, now, to the claims, applicant has amended the claims so they are now limited to selecting a bank for access based on the burst rate programmed into a mode register. Specifically, claim 1 now specifies that the claimed memory device includes a mode register that may be programmed to select the length of data bursts when the memory device is operating in a burst mode. The claim further specifies that the mode register causes bank control logic to select the bank to which data are to be written or from which data are to be read based upon the length of data burst programmed in the mode register. As explained above, none of the cited references, whether taken alone or in combination, disclose or suggest using the burst length programmed into a mode register to select the memory bank being accessed so that the task of selecting a memory bank of proper size can be accomplished internally within the memory device.

Amended claim 11 is directed to a memory subsystem containing a memory device having a mode register that may be programmed to select the length of data bursts when the memory device is operating in a burst mode. As explained above, the use of a mode register for this purpose is admittedly conventional. However, claim 11 further specifies that the memory device is operable to select the bank to which data are to be written or from which data are to be read based on the length of data bursts programmed in the mode register. As a result, the system controller used in the claimed memory subsystem need not be specially adapted to select different banks based on the characteristics of a device seeking access to the memory device or based on other factors that are external to the memory device. Instead, the mode register in the claimed memory device can be programmed to select a burst length in a conventional manner, and doing so causes the memory device itself to select a memory bank of proper size. As explained above, a memory bank of the proper size is assigned in the Lee memory device by and address generated by a device external to the memory device based on the characteristics of a master device seeking access to the memory device.

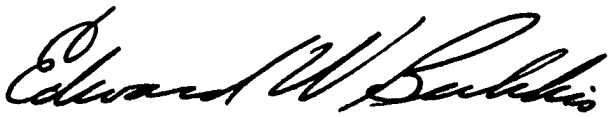
Amended claim 21 is directed to a computer system using the same memory device that is used in the memory subsystem of claim 11. Claim 21 is therefore patentable for at least the same reasons that claim 11 is patentable.

Applicant has also amended claim 8 to obviate the informalities noted in the Office Action.

All of the claims remaining in the application as amended are now clearly allowable. Favorable consideration and a timely Notice of Allowance are therefore earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



Edward W. Bulchis
Registration No. 26,847
Telephone No. (206) 903-8785

EWB:dms

Enclosures:
Postcard
Check
Fee Transmittal Sheet (+copy)
Supp. IDS, Form PTO-1449

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)

h:\ip\clients\micron technology\1200\501256.01\501256.01 amend oa 100505.doc